WHAT IS CLAIMED IS:

1. A frequency synthesizer comprising;

an input node for receiving a reference frequency signal;

a variable oscillator having a first control input and a second control input, and producing an oscillator output signal whose frequency is dependent on said first and second control inputs;

an analog voltage phase detector having a first phase-detection input responsive to said reference frequency signal and a second phase-detection input responsive to said oscillator output signal from said variable oscillator, said analog voltage phase detector being effective for producing a first control signal indicative of a phase difference between said reference frequency signal and said oscillator output signal, said first control signal being coupled to said first control input of said variable oscillator, wherein an analog loop is defined by the signal path along said first control signal from said analog voltage phase detector to said variable oscillator and along said oscillator output signal from said variable oscillator back to said analog voltage phase detector;

a digital frequency difference detector having a first frequency-detection input responsive to said reference frequency signal and a second frequency-detection input responsive to said oscillator output signal, said digital frequency difference detector being effective for producing a second control signal indicative of a frequency difference between said reference frequency signal and said oscillator output signal, said second control signal being coupled to said second control input of said variable oscillator, wherein a digital loop is defined by the signal path along said second control signal from said digital frequency difference detector to said variable oscillator and along said oscillator output signal from said variable oscillator back to said digital frequency detector;

wherein the bandwidth of said analog loop is greater than the bandwidth of said digital loop.

2. The frequency synthesizer of claim 1, wherein the bandwidth of said analog loop is at least 200 times greater than the bandwidth of said digital loop.

3. The frequency synthesizer of claim 1, wherein said variable oscillator is a voltage controlled oscillator.

4. The frequency synthesizer of claim 1, further comprising a filter, wherein said first control signal is coupled to said first control input via said filter.

5. The frequency synthesizer of claim 1, further comprising a first frequency divider, wherein:

said input node for receiving said reference frequency signal is coupled to an input of said first frequency divider, and the output of said first frequency divider is coupled to said first phase-detection input of said analog voltage phase detector, whereby the first phase-detection input of said analog voltage phase detector is responsive to said reference frequency signal via said first frequency divider.

6. The frequency synthesizer of claim 5, wherein the output of said first frequency divider is coupled to said first frequency-detection input of said digital frequency difference detector, whereby the first frequency-detection input of said digital frequency difference detector is responsive to said reference frequency signal via said first frequency divider.

7. The frequency synthesizer of claim 1, further comprising a second frequency divider having an input coupled to receive said oscillator output signal from said variable oscillator, and having an output coupled to said second phase-detection input of said analog voltage phase detector, whereby the second phase-detection input of said analog voltage phase detector is responsive to said oscillator output signal via said second frequency divider.

8. The frequency synthesizer of claim 7, wherein the output of said second frequency divider is further coupled to said second frequency-detection input of said digital frequency difference detector, whereby the second frequency-

detection input of said digital frequency difference detector is responsive to said oscillator output signal via said second voltage divider.

9. The frequency synthesizer of claim 1, wherein said second control signal from said digital frequency difference detector is coupled to said second control input of said variable oscillator via a digital-to-analog converter that provides said second control input an analog representation of the digital output from said digital frequency difference detector.

10. The frequency synthesizer of claim 9, wherein said variable oscillator includes a summer for summing together the control signals at its first and second control inputs to produce a composite frequency control signal.

11. The frequency synthesizer of claim 1, wherein the variable oscillator's first and second control inputs are independent of each other, and said variable oscillator has at least first and second frequency adjusting mechanisms separately responsive to said first and second control inputs, respectively.

12. The frequency synthesizer of claim 11, wherein said first frequency adjusting mechanism includes a varactor responsive to said first control input, and wherein said second frequency adjusting mechanism includes at least one capacitor conditionally coupled and decoupled from said variable oscillator in response to said second control input.

13. The frequency synthesizer of claim 1, wherein said digital frequency difference detector includes:

an n-bit counter for counting pulses received at said first frequency-detection input, whereby said n-bit counter maintains a pulse-count of said reference frequency signal;

an m-bit counter for counting pulses received at said second frequency detection input, whereby said m-bit counter maintains a pulse-count of said oscillation output signal, and wherein m is greater than n;

a first memory cell for storing a SET condition in response to the n^{th} bit within said m-bit counter transitioning into a first logic state and for maintaining said SET condition irrespective of said n^{th} bit within said m-bit counter transitioning out of said first logic state;

a second memory cell for storing a SET condition in response to the $(n+1)^{th}$ bit within said m-bit counter transitioning into said first logic state and for maintaining said SET condition irrespective of said $(n+1)^{th}$ bit transitioning out of said first logic state;

wherein said n-bit counter and said m-bit counter are halted in response to the n^{th} bit within said n-bit counter transitioning into said first logic state; and

wherein upon said halting of said n-bit and m-bit counters, said digital frequency difference detector determines:

a) that the output frequency of said variable oscillator is lower than said reference frequency signal if neither of said first or second memory cells have said SET condition stored; or

b) that the output frequency of said variable oscillator is higher than said reference frequency signal if said second memory cell has said SET condition stored; or

c) that the output frequency of said variable oscillator is higher than said reference frequency signal if said first memory cell has said SET condition stored and any bit within said m-bit counter excluding a predetermined number of least significant bits is set to said first logic state; or

d) that the output frequency of said variable oscillator is locked to said reference frequency signal if said first memory cell has said SET condition stored and said second memory cell does not have said SET condition stored and no bit within said m-bit counter excluding said predetermined number of least significant bits is set to said first logic state.

14. The frequency synthesizer of claim 13, wherein said predetermined number of least significant bits is one, whereby upon the halting of said n-bit and m-bit counters, said digital frequency difference detector determines that the output frequency of said variable oscillator is higher than said reference frequency signal if said first memory cell has said SET condition stored and any bit higher than the first bit within said m-bit counter is set to said first logic state.

15. The frequency synthesizer of claim 13, wherein:

said first and second memory cells are first and second latches, respectively;

said first and second latches store said SET condition by being set to, i.e. latching-in, said SET condition; and

said first and second latches may selectively remove said SET condition by being set to a RESET condition.

16. The frequency synthesizer of claim 15, wherein said first and second latches are set to said SET condition by latching-in one of a logic high state and a logic low state, and are set to said RESET condition by latching-in the other of said logic high state and logic low state opposite said SET condition.

17. The frequency synthesizer of claim 15, wherein said digital frequency difference detector further includes a control logic circuit, and wherein:

said first latch is reset in response to said control logic circuit;

said second latch is reset in response to said control logic circuit; and

said first and second latches are reset following the determination of whether the output frequency of said variable oscillator is lower than, greater than, or locked to said reference frequency signal.

18. The frequency synthesizer of claim 17, wherein said digital frequency difference detector further includes:

a first masking gate responsive to said control logic circuit and effective for selectively coupling and decoupling said first frequency-detection input to and from said n-bit counter as determined by said control logic circuit, wherein said n-bit counter counts pulses received at said first frequency-detection input when said first masking gate couples said first frequency-detection input to said n-bit counter, and ceases to count pulses received at said first frequency detection input when said first masking gate decoupled said first frequency-detection input from said n-bit counter whereby said n-bit counter is halted; and

a second masking gate responsive to said control logic circuit and effective for selectively coupling and decoupling said second frequency-detection input to and from said m-bit counter as determined by said control logic circuit, wherein said m-bit counter counts pulses received at said second frequency-detection input when said second masking gate couples said second frequency-detection input to said m-bit counter, and ceases to count pulses received at said second frequency detection input when said second masking gate decoupled said second frequency-detection input from said m-bit counter whereby said m-bit counter is halted.

19. The frequency synthesizer of claim 17, wherein said digital frequency difference detector further includes an up/down counter, and said control logic circuit instructs said up/down counter to:

make a count step change in one of an up or down direction if the output frequency of said variable oscillator is determined to be higher than said reference frequency signal,

make a count step change in the other of said up or down direction if the output frequency of said variable oscillator is determined to be lower than said reference frequency signal, or

remain unchanged if the output frequency of said variable oscillator is determined to be locked to said reference frequency signal;

wherein the output of said up/down counter is coupled to said variable oscillator.

20. The frequency synthesizer of claim 19, wherein:

the output frequency of said variable oscillator is dependent on the enabling or disabling of multiple capacitors and each of said multiple capacitors is enabled and disabled in response to a respective cap_control input, and

said up/down counter places its current count value on an output bus, said output bus constituting said second control signal, wherein separate bits in said output bus are coupled to separate cap_control inputs to modify the frequency of said variable oscillator.

21. The frequency synthesizer of claim 19, wherein:

the output frequency of said variable oscillator is dependent on the signal strength of a frequency-adjust-input coupled to receive said second control signal;

the output of said up/down counter is applied to a digital-to-analog converter to produce said second control signal.

22. The frequency synthesizer of claim 19, wherein:

said digital frequency difference detector provides an inherent low pass filter for filtering the frequency difference between the reference frequency signal and the oscillator output signal from said variable oscillator; and

the bandwidth of said inherent low pass filter is adjustable by increasing or decreasing the value of n in said n-bit counter and adjusting the increment/decrement step size of said up/down counter.